IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)
e-ISSN: 2278-2834,p- ISSN: 2278-8735.
PP 93-99
www.iosrjournals.org

Effect of Process Parameters Variation on Dual Material Gate SOI Junctionless Transistor.

S.C.Wagaj[1] , Y.V.Chavan[2],Sr IEEE-Member
Dept of Electronics & Telecommunication JSPM's RSCOE Tathawade Pune, MS-India
Savitribai Phule Pune University, Pune
scwagaj@yahoo.com chavan.yashwant@gmail.com

ABSTRACT : *All existing transistors contents semiconductor junctions. A distance between junctions in modern device drops below 10nm, then high doping concentration gradients become necessary. Law of diffusion and statistical nature of the distribution of the dopant atoms, such junctions represent an increasingly difficult fabrication challenge for the semiconductor industry. Here, in this paper present junctionless transistors and Dual material gate silicon on Insulator Junctionless Transistor (DMG SOI JLT) is proposed in this paper. Its characteristics is demonstrated & compared with a single Material gate SOI JLT using EDA tools used for simulation. The result shows that the DMG-SOI JLT has a number of desirable features, such as high on state current. The potential distribution of DMG SOI JLT has an abrupt change the transition of two gates and enhances the electric field in the channel.*

Keywords - *Double Gate Junctionless Transistor(DGJLT); Bulk Planner Junctionless Transistor(BPJLT);Duble Material Gate- Double Gate Junctionless Transistor(DMG-DGJLT);Gate All Around Junctionless Transistor(GAA JLT) ;*

I. INTRODUCTION

The scaling of gate length in the bulk MOSFETs, then efficiency of the gate control decreases in the channel. In order to overcome this limitation, various device structures such as fully depleted SOI FETs as well double gate and multiple gates FET have been proposed [2], due to ability to suppress short channel effects. In such devices, however ultra-shallow source/drain junction fabrication is becoming one of the main in view of the required process steps and related thermal budget. However, the formation of ultra sharp junctions between source drain and channel becomes complex when the channel length of classical multigate MOS transistors is scaled down to extreme dimensions. A solution to this problem in the form of novel structure called "Junctionless multi gate transistor" [2]-[5].Junction less transistors have been considered as best candidate for the continuation of moors law and reduced electric field perpendicular to the channel[3]. Junctionless transistor can be described as a device which is heavily doped, and where the type of doping in the channel region is the same as source and drain regions. The device is fully turned on when operating at flatband condition, and turned off by full depletion of its channel region, whereby this depletion is caused by the work function difference between the gate material and doped channel region of the device. The loss gate control over channel charges observed in very short channel transistors. For this problem gate alternative technologies, such as multigate architecture [6]-[7]. The presence of gate control on more than one side of the device effectively improves the electrostatic control over the channel, reducing short channel effects [1]. Especially the operation of JLT devices is quite different the standard inversion (IM) transistors. Indeed it is based on bulk conduction suspended to reduce surface roughness scattering [33]. However, there are also several issues related to the channel doping and bulk mobility degradation and the variability of both threshold voltage and drain induced barrier lowering. The impact ionization occurs at the surface inversion layer in IM transistor but the bulk impact ionization occurs in the conduction channel in a JL transistor. Surface impact ionization occurs at the drain voltages ˜ 40% higher than the bulk impact ionization; a large supply voltage is required for impact ionization in IM transistors [16]. The advantage of JL transistor also include: 1) lower leakage current 2) high I_{on}/I_{off} ratio 3) lesser sub threshold slope and variability [5].However, it is difficult to fully deplete the channel region of JL transistor by utilizing the single gate control [3][4[].Use of high-k spacers or the combination of high and low-k spacers for improves more of the device on-state performance than the electrostatic integrity. JLTs operate at high vertical electric filed in the channel in off state and low filed in on-state. JLT transistors with high-k spacers, which can improve electrostatic integrity of the device and potentially making the device scalable to extremely short channel length [15]. It was observed that the use of a high-k dielectric as a spacer brings an improvement in the off state current. However, the on-state current affected by dielectric constant of spacer. Effect of spacer width on device performance. When increasing spacer width on state current marginally decreases and off state current

marginally increases. Hfo_2 as spacer dielectric offer highest I_{on}/I_{off} ratio [12]. Dual material (DMG) devices offer improved carrier transport efficiency [21], trans conductance and the drain output resistance compared with single-material-gate (SMG) conventional MOSFET [10-12]. Lou et.al have reported that in a DMG Junctionless Nanowire Transistor, out of different combination of L_{M1} & L_{M2}, $L_{M1}/L=1/2$ & work function difference=0.5 give overall best characteristics [13]. Junction less nanowire field effect transistor such as the Gate-All-around architecture are potential candidates for next generation high speed and low power electron devices owing to their electrostatic integrity and simple fabrication steps, still maintaining acceptable current densities[8].The variability of the threshold voltage [32] due to fluctuation of the channel dimension was reduced by increasing the number of gate electrodes coming into contact with each channel surface in multiple gate devices[23].

II. JUNCTIONLESS DOUBLE GATE FIELD EFFECT TRANSISTOR

The main conduction mechanism in a junctionless Field-effect transistor (JLFET) relies not on the surface but on the bulk current; moreover, it turns off by making the channel fully depleted [1].Utilizing a single gate, it is rather difficult to fully deplete the channel, and acceptable threshold voltage are also difficult to obtain under such condition [3].Therefore, a double gate (DG) structure is a promising candidate for JLFETs due to its good electrostatic control of the channel [22].

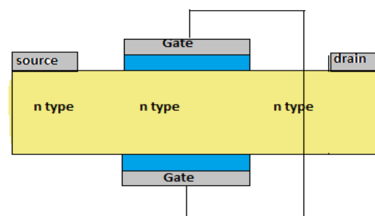

Fig-1 Schematic diagram of JL Double Gate (DG) MOSFET [22].

Fig.1 presents schematic view of Double gate of Junctionless transistor. This structure presents a real advantage since its fabrication process is simplified compared to the conventional process (there are no doping gradients in the device and no semiconductor type inversion). I have studied that JL DG-FET characterized by a higher bipolar gain than IM-DGFET, due to stronger floating body effect [27]. The main reason for low driving current in case of junctionless transistor is mainly due to the degraded electron mobility because of unavoidable high channel doping concentration [22]. The difference in electron velocity along the lateral position between conventional and junctionless DG-MOSFET indicating very low values of drain current in junctionless transistor compared to conventional transistor. The transconductance of G_m of the junctionless nMOSFET is also significantly lower than that of conventional DG-MOSFET for the same gate voltage V_g. Junction less MOSFETs exhibits slower degradation of G_m compared to conventional MOSFET which can be well explained by the fact that the reduction mobility with gate voltage [18].D.Munteanu et.al indicate that JL-DGFET SRAMs are naturally more immune to radiation than FDSOI SRAMs, but more sensitive to radiation than IM-DGFET SRAMs [28].

III. MULTIGATE JL FET

Fig.2 presents bird eye's view of a MuGFETs. The junctionless MuGFETs have better short channel characteristics than inversion mode devices [6]. In a multigate FET the gate electrode is wrapped around a silicon wire, called finger or fin forming a gate structure that delivers optimal control.

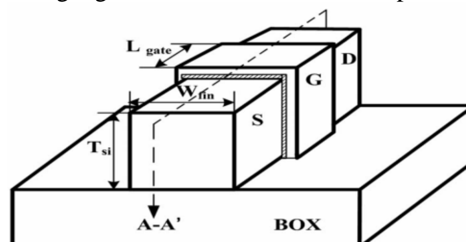

Fig.2 3D View of gated resistor [6]

Channel is controlled electrostatically by the gate from multiple sides; channel is better controlled by the gate than conventional MOSFET.This provides greater voltage gain, which is useful for analog circuit. Multigate device is improved on-state drive current therefore fast circuit speed [11].Early voltage V_{EA} and A_V are more

sensitive to W_{fin} variation in junctionless devices than in inversion mode transistors. Junctionless transistors are able to provide a constant drain current over a wide temperature range. The different behavior observed between IM and JL devices as a function of temperature can be attributed to the lower variation of mobility with temperature in junctionless transistor [11].In JL devices mobility almost independent of temperature. These effects explain the continuous increase in on current with temperature in JL MuGFET [24].The influence of temperature on the intrinsic voltage gain of the device is addressed in Fig.4 for IM and JL devices with W_{fin}, mask of 30 and 40nm of V_{DS}=1V.IM devices present maximum gain at room temperature, whereas A_V always increases with T in JL transistor [7].The bulk planner junctionless transistor (BPJLT) is a source-drain-junction free transistor accompanied with junction isolation. It is junctionless in the source-channel-drain path but needs a junction for vertical direction for isolation purpose. The advantage of BPJLT over existing transistor are i) The full compatibility to industry standard ii) Lower cost iii) Better scalability. The device advantages low thermal budget after gate formation [29].In BPJLT has uniform lateral doping i.e. the source, drain and the channel has identical doping. In the on state, the SOI-JLT device is uniformly in flatband, whereas for the BPJLT a fraction of the device layer at the top-corresponding to the effective device layer-is in flatband the rest of it still remaining depleted [29]. The thinner effective is in the case of the BPJLT suggests that it would exhibit better electrostatic integrity than the SOI-JLT. BPJLT has superior I_{ON}/I_{OFF}, smaller drain-induced-barrier-lowering (DIBL) and subthreshold slope. This establishes the superior electrostatic integrity. Device with high-k spacer [15] show a reduced off-state leakage current. As the dielectric constant of spacer increases, the slope of the I_D-V_{GS} increases by using appropriate gate metal work function, the improvements gained in the leakage current can be traded for higher ON current for the device using high-k spacers. The junction isolation of BPJLT would however come with a capacitance that could increase the delay of operation [29]. The Gate-All-Around junctionless transistor devices showed excellent characteristics with the aid of the GAA and junction free nature. The variability of the threshold voltage due to fluctuation of the channel dimension was reduced by increasing the number of gate electrodes coming into contact with each channel surface in multiple gate devices [23].The typical transfer and output characteristics of the fabricated All-Around-Gate (AAG) junctionless transistor with the oxide/nitride/oxide gate dielectric. The transfer characteristics show good dc performance levels with an on/off ratio that exceeds 10^5 and good gate controllability even with an EOT of 13nm, L_G=50nm. The variation of the electric field at the drain end of JLDMDG (Junctionless Dual Material Double Gate) MOSFETs is much smaller than that of JLSMDG (Junctionless Single Material Double Gate) MOSFETs as the drain bias increases. The electric field distributions of the JLDMDG MOSFETs ensure better average electric field across the channel and suppress the Hot Carrier Effect (HCE) by the high drain voltage [17].

IV. Proposed Device structure Dual Material Gate Silicon on Insulator Junctionless Transistor (DMG SOI JLT) and simulation

The device structure for an n-type DMG SOI JLT is shown in Fig.3.An n type DMG SOI JLT has homogeneous (N^+) and uniform doping for the source, channel, and drain region. P^+ polysilicon is used as gate material.

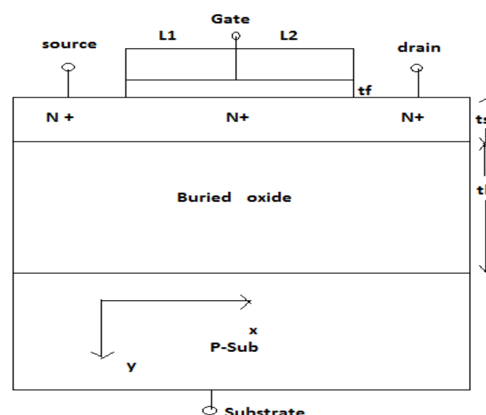

Fig.3 cross sectional view of n-type DMG SOI Junctionless Transistor

The operation of DMG is explained in [6]. A DMG SOI JLT has two metal gates, M_1 and M_2 resectively.Recently, Lou et.al.[15] have reported that in a DMG JLT, out of different combination of $L_{M1}$and L_{M2}, L_{M1}/L=1/2 and work function difference give the overall best characteristics of the device. However, the

effects of the DMG structure have not been studied so far in case of SOI Junctionless MOSFETs, which play an important role in the present day CMOS design. For DMG SOI JLT device, W_{M1} and W_{M2} are set to be 5.14eV and 4.4eV respectively which correspond to acceptable threshold voltage for device. We have kept L_{M1}:L_{M2}=20:20nm, buried oxide 360nm and channel thickness 10nm for DMG SOI JLT.The device are optimized by adjusting channel doping concentration (N_D) values as to have threshold voltage (V_T) of 0.196V.The aim of this paper is, therefore to study for the potential, electric field benefits offered by the DMG gate in suppressing the SCEs in SOI JL MOSFETs.

TABLE 1: Process/Device Parameters

Parameters	SMG SOI JLT	DMG SOI JLT
L(nm)	40	40
L_{M1}:L_{M2}(nm)	-	20:20
W_{M1}:W_{M2}(eV)	4.1	4.77:4.1
N_D(cm^{-3})	0.4e18	0.4e18
T_{OX}(nm)	1(sio2)	1(sio2)
T_{si} (nm)	10	10

Fig.4 shows the potential distributions along the channel direction at drain voltage(V_{DS})=0.5V,1V and 1.5V and gate voltage V_{GS} of 0 to 1V. The potential distribution of DMG have abrupt change on the workfunction transition point from W_{M1} and W_{M2}, whereas SMG SOI JLT follows a monotonous trend from source and drain. The abrupt change is caused by the different gate workfunction.

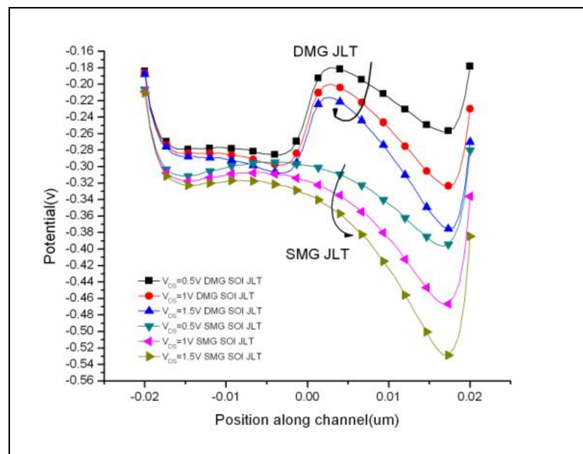

Fig.4 Potential distribution of DMG SOI JLT and SMG SOI JLT along the channel with V_{DS}=0.5,1,1.5V, L=40nm. Tsi =10nm. t_{ox}=1 nm.

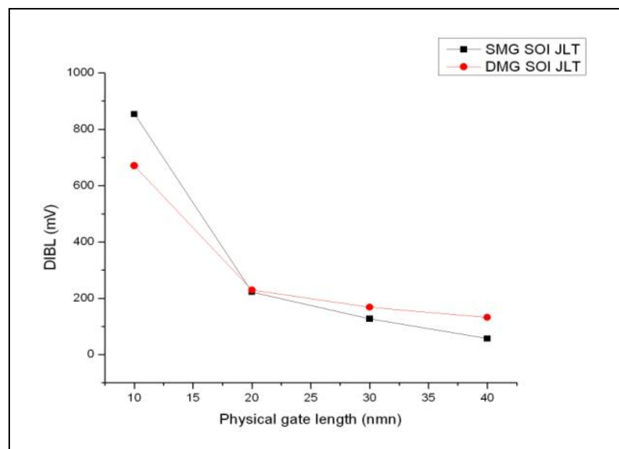

Fig.5 DIBL at VDS=50 mV in DMG SOI JLT and SMG SOI JLT devices with Tsi=10nm

Fig.5 shows the result for DIBL and threshold voltage versus physical gate length [19] for both DMGSOI JLT and SMG SOI JLT. Drain Induced Barrier Lowering means threshold voltage difference when V_{DS}=0.05V and V_{DS}=1V.[DIBL=V_{th} (V_{DS}=0.05V)-V_{th}(V_{DS}=1V)].DMG SOI JLT's improve the performance compare to SMG SOI JLT when channel length reduces. A DIBL =671mV/V is achieved at L_G=10nm for DMG SOI JLT and DIBL=854 mV/V for SMG SOI JLT. A DIBL =229mV/V is achieved at L_G=20nm for DMG SOI JLT and DIBL=222 mV/V for SMG SOI JLT. A DIBL =168mV/V is achieved at L_G=30nm for DMG SOI JLT and DIBL=127 mV/V for SMG SOI JLT. A DIBL =132mV/V is achieved at L_G=40nm for DMG SOI JLT and DIBL=57 mV/V for SMG SOI JLT.

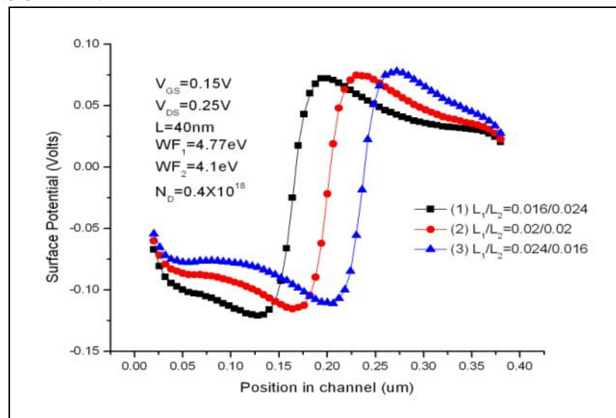

Fig.6 Variation of surface potential with position in channel for different combination of gate lengths L_1 and L_2, keeping the sum (L_1+L_2) constant.

Fig.6 shows the variation of surface potential with the channel position for different combinations of gate length L_1 and L_2 of M_1 and M_2, respectively [21]. Keeping the sum of total gate length, (L_1+L_2), to be constant.

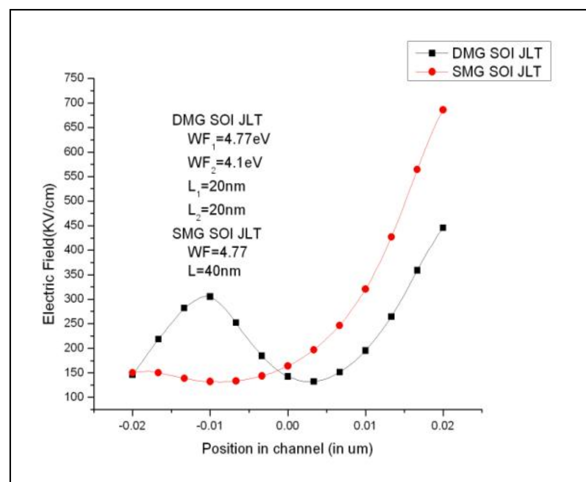

Fig.7 Longitudinal electric field along the channel toward the drain end obtained from the TCAD simulation in DMG SOI and SMG SOI JLT with a channel length L=40nm and drain bias V_{DS}=1.75V. The parameters used are V_{GS}=0.15V, t_{ox}=1nm, t_b=360nm,t_{si}=10nm,V_{SUB}=0V, N_D=0.4X10^{18} cm^{-3}.

It is seen from the figure that the position of minimum surface potential, lying under M1 is shifting toward the source as the length of gate M_1 is reduced [13]. This causes the peak electric field in the channel to shift more toward the source end and thus there is a more uniform electric field profile in the channel. In the Fig 7 it is seen that to enhance the electric field of SMG and DMG SOI JLT, for SMG SOI JLT, there is only one peak near the drain. The DMG SOI JLT much lower electric field peak near the drain side compared with SMG SOI JLT indicating that it suppresses SCE and hot carrier effect more effectively.

V. CONCLUSION

The objective of this paper was to presents study of junctionless transistors.

-In junctionless transistor due to dual material gate improve the carrier transport efficiency.

-The work function difference significantly affects the characteristics of devices by changing the channel control ability and the screening effect.
-drive current capability of the device and Peak value of electric field near the drain side for the DMG SOI JLT improves
- The Short channel effect and hot carrier effect of Junction fewer Transistors reduces.

It seems that the DMG SOI JLT can be a better candidate for better performance and implementation in semiconductor industries.

ACKNOWLEDGMENT

The authors would like to thank the precious support of Dr.D.S.Bormane Principal JSPM's Rajarshi Shahu college of Engineering Pune, Research centre of Savitribai Phule Pune University Pune.

REFERENCES

[1] Colinge JP, Lee CW, Afzalian A, Akhavan ND, Yan R, Ferain I, et al"Nanowire transistors without junctions.",Nat. Nanotechnol. 2010;5:225–9.
[2] Chi Woo lee,Aryan Afazalian, Nima Dehdashti, Ran Yan,J.P.Colinge,"Junctionless Multigate Field Effect Transistor",Applied Physics Letters 94,053511 (2009).
[3] J.P.Colinge, Chi-woo lee, Isabelle Ferain, Nima Dehdashti,Ran Yan, Pedram Razavi,"Reduced electric Field in Junctionless Transistors", Applied Physics Letters 96, 073510 (2010).
[4] D.Y.Jeon, S.J.Park,M.Mouis,S.Barraud,G.T.Kim,G. Ghibaudo,"A new method for the extraction of flatband voltage and doping concentration in Trigate Junctionless Transistor", solid state Electronics 81(2013) 113-118.
[5] C.-W. Lee, A. N. Nazarov, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, *et al.*, "Low subthreshold slope in junctionless multigate transistor," *Appl. Phys. Lett.*, vol. 96, no. 10, pp. 102106-1–102106-3, Mar. 2010.
[6] C.-W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, *et al.*, "Performance estimation of junctionless multigate transistors," *Solid State Electron.*, vol. 54, no. 2, pp. 97–103, Feb. 2010.
[7] R. T. Doria, M. A. Pavanello, R. D. Trevisoli, M. de-Souza, C.-W. Lee, I. Ferain, *et al.*, "Junctionless multiple-gate transistors for analog applications," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2511–2519, Aug. 2011.
[8] M.Li,K.H.Yeo,S.D.Suk,Y.Y.Yeoh,D.W.Kim,T.Y.Chung,K.S.oh and W.S.Lee,"Sub-10nm gate-all-around CMOS nanowire transistors on bulk si substrate", in VLSI Tech. Dig., 2009, pp.123-135.
[9] S. Cho, K. R. Kim, B.-G. Park, and I. M. Kang, "RF performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1388–1396, May 2011.
[10] P. Razavi and A. A. Orouji, "Dual material gate oxide stack symmetric double gate MOSFET: Improving short channel effects of nanoscale double gate MOSFET," in *Proc. 11th Int. Biennial BEC*, Oct. 2008, pp. 83–86.
[11] W. Long, H. Ou, J.-M. Kuo, and K. K. Chin, "Dual-material gate (DMG) field effect transistor," *IEEE Trans. Electron Devices*, vol. 46, no. 5, pp. 865–870, May 1999.
[12] P. Kasturi, M. Saxena, M. Gupta, and R. S. Gupta, "Dual material double-layer gate stack SON MOSFET: A novel architecture for enhanced analog performance—Part I: Impact of gate metal workfunction engineering," *IEEE Trans. Electron Devices*, vol. 55, no. 1,pp. 372–381, Jan. 2008.
[13] H. Lou, L. Zhang, Y. Zhu, X. Lin, S. Yang, J. He, *et al.*, "A junctionless nanowire transistor with a dual-material gate," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1829–1836, Jul. 2012.
[14] Chi woo lee, J P Colinge,"Junctionless Multigate Field Effect Ttansistor",*Applied Physics letters* 94,053511 (2009).
[15] S. Gundapaneni, S. Ganguly, and A. Kottantharayil, "Enhanced electrostatic integrity of short-channel junctionless transistor with high-k spacers," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 261–263, Mar. 2011.
[16] R. K. Baruah and R. P. Paily, "Impact of high-k spacer on device performance of a junctionless transistor," *J. Comput. Electron.*, vol. 12, no. 1, pp. 14–19, Mar. 2013.
[17] Ping wang,Yigi zhuang,"Subthreshold behavior models for nanoscale junctionless Double gate MOSFETs with dual material gate stack",*japanese journal of applied physics* 53, 084201 (2014).
[18] P. Kasturi, M. Saxena, M. Gupta, and R. S. Gupta, "Dual material double-layer gate stack SON MOSFET: A novel architecture for enhanced analog performance—Part II : Impact of gate-dielectric material engineering," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 382–387, Jan. 2008
[19] C Onal, R.woo,H.Y.serene koh, P.B.Griffin, and J.D.Plummer,"A novel delpletion-IMOS (DIMOS) device with improved reliability and reduced operating voltage", *IEEE Electron Device Lett*.Vol-30, no-1, pp.64-67, jan 2009.
[20] Seung min lee and Jang Tae park,"The impact of substrate Bias on the steep subthreshold slope in Junctionless MuGFETs", *IEEE Transaction on Electron Devices*, Vol.60, No-11,November 2013.
[21] M. J. Kumar and A. Chaudhry, "Two-dimensional analytical modeling of fully depleted DMG SOI MOSFET and evidence for diminished SCEs,"*IEEE Trans. Electron Devices*, vol. 51, no. 4, pp. 569–574, Apr. 2004.
[22] K P Pradhan, S.K.Mohapatra, P.K.Agarwal,"Symmetric DG-MOSFET with gate and channel Engineering:A 2-D simulation study", Microelectronics and solid state Electronics(scientific and academic pub publication Microelectronics and solid state Electronics(scientific and academic publication, Vol.2,issue.1, PP.1-9,Feb 2013.
[23] Dong-I1 Moon,Sung-Jin choi, Juan Pablo Duarte and Yang-kyu choi,"Inverstigation of silicon Nanowire Gate-All-Around Junctionless Transistor Built on aBulk Substrate", *IEEE Transaction on Electron Devices,* Vol.60,No-4,April 2013.
[24] Chi-woo Lee,Adrien Borne,Isabelle Ferain,Aryan Afzalian, Ran Yan,"High-Temperature of silicon junctionless MOSFETs",*IEEE Transction on Electron Devices,* Vol-57,No-3,March-2010.
[25] Sung-Jin Choi, Dong I1 Moon,Sungho kim,Jae-Hyuk Ahn,Jin-seong Lee,Jee-Yean Kim, Yang-kyu choi,"Nonvolatile memory by All-Around-Gate Junctionless Transistor Composed of silicon Nanowire on Bulk Substrate",*IEEE Electron Devices Letters*, Vol-32,No.5,May 2011.

[26] Yi Song,Chen zhang,Ryan Dowdy,Kelson Chabak,Parsian K.Mohseni,"III-V Junctionless Gate-All-Around Nanowire MOSFETs for High Linearity Low Power Applications", *IEEE Electron Devices Letters*, Vol.35,No-3, March 2014.
[27] Munteanu D, Autran JL, "3-D numerical simulation of bipolar amplification in junctionless double-gate MOSFETs under heavy-ion irradiation", *IEEE Transaction Nucl Sci* 2012; 59(4): 773-80.
[28] D.Munteanu, J.L.Autran,"Radiation sensitivity of Junctionless double gate 6T SRAM cells investigated by 3-D numerical simulation", Microelctronics Reliability 54(2014) 2284-2288.
[29] Suresh Gundapaneni,Mohit Bajaj,Rajan Pandey,Swaroop Ganguly, Anil Kottantharayil,"Effect of Band-to-Band Tunneling on junctionless Transistors",*IEEE Transaction on Electron Devices*, Vol.59,No-4, April 2012.
[30] R.K.Baruah and R.P.Paily," Imapact of High-k spacer on device performance of a junctionless transistor", J.Compute. Electron., Vol.12, no.1, pp.14-19, Mar.2013.
[31] T.Rudenko,A.Nazarov,R.Yu,S.Barraud,K.Cherkaoui,P.Razavi,G.Fagas,"Electron mobility in heavily doped junctionless nonowire SOI MOSFETs", Microelectronics Engineering 109(2013) 326-329.
[32] Y.V. Chavan, D.K. Mishra, "Modeling of the Photo-detectors for Computer Vision System", published in the International the Journal of optics by the Springer Publication, Vol 39, (4), Dec.2010, pp. 149-156,
[33] Y. V. Chavan, D. K. Mishra, "Improved CMOS Digital Pixel Sensor", presented at the National Conference on Wireless Communication and Networking organized by L&T., Powai on 9 - 10 Dec. 2008.